



# Data Modeling for Hardware Component Information in Testbeds

## Motivation

At the Chair of Network Architectures and Services, we host various testbeds for network experiments. We employ a self-developed testbed methodology called "pos" to conduct our experiments. This methodology documents all relevant data and metadata associated with each experiment. Alongside experimental data, recording the hardware components of the experiment hosts is crucial for comprehensive documentation. This hardware information simplifies the reproduction of experiments and ensures consistent results.

Currently, we use a proprietary JSON-based format to describe hardware information. As part of our commitment to open science, we aim to explore how YANG—known for its ability to offer a standardized and machine-readable representation of data—can enhance the management and understanding of the hardware used in our experiments. Yet Another Next Generation (YANG), standardized in RFC 6020, is a data modeling language designed for the NETCONF and RESTCONF protocols. In recent years, many data models for various use cases have been proposed.

Hostname	Access Group	Processor	Cores	Memory	Network Interface
ada	lab_testing	AMD EPYC 7542 AMD EPYC 7542	64	1024	Intel 82599ES 10-Gigabit SFI/SFP+ Intel E810-C for QSFP Intel E810-C for QSFP Intel E810-XXV for SFP Intel E810-XXV for SFP Intel X550 Intel XXV710 for 25GbE SFP28
alqof1	alqofand Microtestbed	AMD EPYC 7543	32	512	Broadm BCM57416 NetXtreme-E Dual-Media 10G RDMA Intel 82580 Gigabit Intel E810-C for QSFP Intel E810-XXV for SFP

Visualization of hardware information on the testbed's website

## Your Task

- Familiarize yourself with YANG (RFC 6020) and the IETF Hardware Model for YANG (RFC 8348)
- Propose/Extend a data model for testbed-specific hardware information
- Implement the data model in our testbed infrastructure
- Demonstrate the functionality in a prototype

## Contact

Eric Hauser hauser@net.in.tum.de

